DATA SHEET

TDA9855
I²C-bus controlled BTSC stereo / SAP decoder and audio processor

Preliminary specification
File under Integrated Circuits, IC02

July 1994

Philips Semiconductors

PHILIPS

I²C-bus controlled BTSC stereo / SAP decoder and audio processor

TDA9855

FEATURES

- Quasi alignment-free BTSC stereo decoder due to auto adjustment of channel separation via I²C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- Audio processor
  - Selector for internal and external signals (line in)
  - Automatic volume level control
  - Subwoofer or surround output with separate volume control
  - Volume control
  - Special loudness characteristic automatically controlled in combination with volume setting
  - Bass and treble control
  - Audio signal zero crossing detection between any volume step switching
- Mute control at audio signal zero crossing
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9855 is a bipolar-integrated BTSC stereo / SAP decoder with hi-fi audio processor (I²C-bus controlled) for application in TV sets.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9855	52	SHDIL	plastic	SOT247AH(1)
TDA9855WP	68	PLCC	plastic	SOT188CG(2)

Note

1. SOT247-1; 1996 December 5.
2. SOT188-2; 1996 December 5.

A license is required for this product. For further information, please contact:

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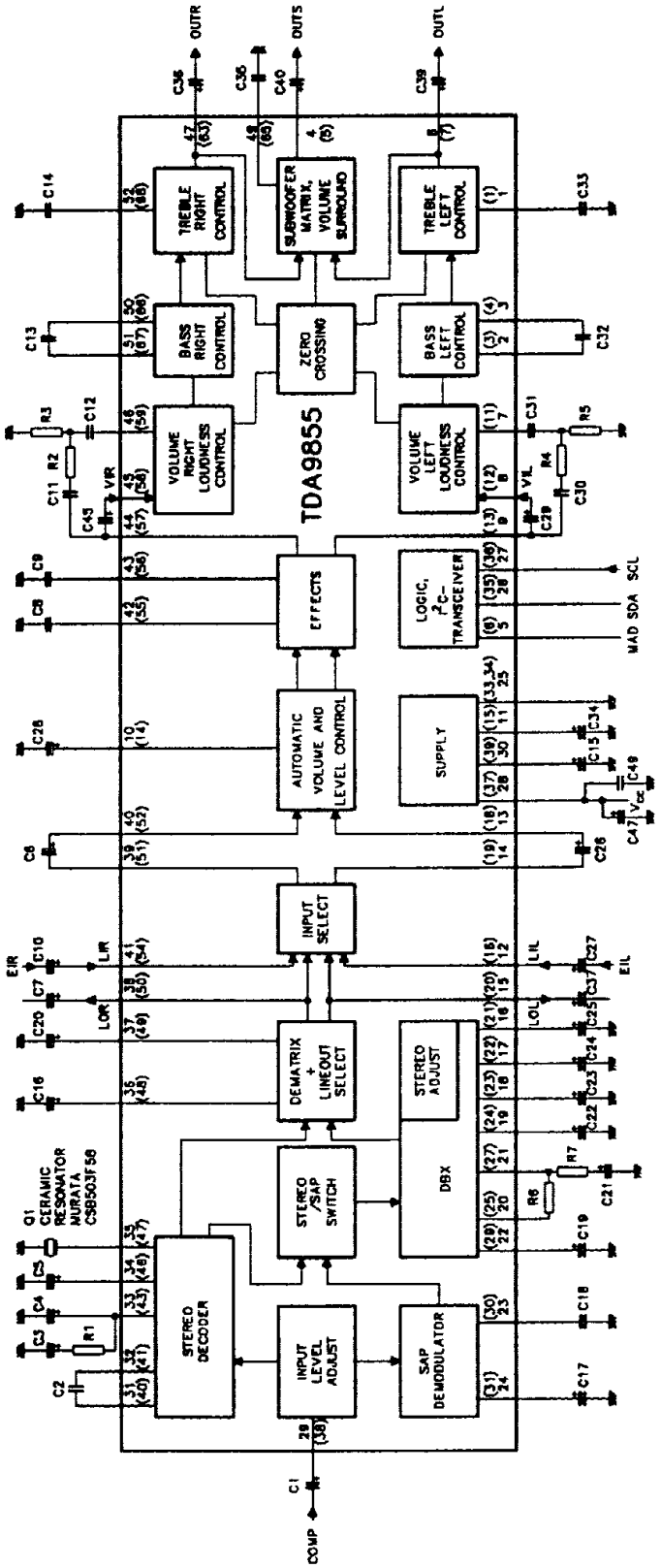


Fig.1 Block, application and test diagram (PLCC pinning in parenthesis).

COMPONENT LIST

elco ±20%; foil or ceramic ± 10%; resistors ±5% unless otherwise specified.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	elco	63 V
C2	470 nF	foil	
C3	4.7 µF	elco	63 V
C4	220 nF	foil	
C5	10 µF	elco	63 V; I_{leak} < 1.5 µA
C6	2.2 µF	elco	16 V
C7	4.7 µF	elco	16 V
C8	15 nF	foil	±5%
C9	15 nF	foil	±5%
C10	2.2 µF	elco	63 V
C11	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C12	150 nF	foil	±5%
C13	33 nF	foil	±5%
C14	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C15	100 µF	elco	16 V
C16	4.7 µF	elco	63 V
C17	4.7 µF	elco	63 V
C18	100 nF	foil	
C19	10 µF	elco	63 V
C20	4.7 µF	elco	63 V
C21	47 nF	foil	±5%
C22	1 µF	elco	63 V
C23	1 µF	elco	63 V
C24	10 µF	elco	63 V ± 10%
C25	10 µF	elco	63 V ± 10%
C26	2.2 µF	elco	16 V
C27	2.2 µF	elco	63 V
C28	4.7 µF	elco	63 V ± 10%
C29	2.2 µF	elco	16 V
C30	8.2 nF	foil or ceramic	±5% SMD 2220/1206
C31	150 nF	foil	±5%
C32	33 nF	foil	±5%
C33	5.6 nF	foil or ceramic	±5% SMD 2220/1206
C34	100 µF	elco	16 V
C35	150 nF	foil	±5%
C36	4.7 µF	elco	16 V
C37	4.7 µF	elco	16 V
C39	4.7 µF	elco	16 V
C40	4.7 µF	elco	16 V

COMPONENT	VALUE	TYPE	REMARK
C45	2.2 μF	elco	16 V
C47	220 μF	elco	25 V
C49	100 nF	foil or ceramic	SMD 1206

COMPONENT	VALUE	REMARK
R1	2.2 KΩ	
R2	20 KΩ	
R3	2.2 KΩ	
R4	20 KΩ	
R5	2.2 KΩ	
R6	8.2 KΩ	±2%
R7	160 KΩ	±2%
Q1	503.5 kHz	MURATA CSB503F58

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{comp}	input signal (RMS value)	100% modulation L + R; f = 300 Hz	–	250	–	mV
V_{LOR}, V_{LOL}	output signal (RMS value)		–	500	–	mV
G_{LA}	input level adjustment control range		–3.5	–	+4.0	dB
α_{st}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L, R}$	total harmonic distortion	f = 1 kHz	–	0.2	–	%
$V_{I, O}$	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G_c	volume control range		–71	–	+16	dB
L_B	maximum loudness boost	f = 40 Hz	–	17	–	dB
G_b	bass control range	f = 40 Hz	–12	–	+16.5	dB
G_t	treble control range	f = 15 kHz	–12	–	+12	dB
G_v	subwoofer control range	f = 40 Hz	–14	–	+14	dB
S/N	signal-to-noise ratio	line out (mono); V_O = 0.5 V (RMS)				
	CCIR noise weighting filter (peak value)		–	60	–	dB
	DIN noise weighting filter (RMS value)		–	73	–	dBA
S/N	signal-to-noise ratio	audio section; V_O = 2 V (RMS); gain = 0 dB				
	CCIR noise weighting filter (peak value)		–	94	–	dB
	DIN noise weighting filter (RMS value)		–	107	–	dBA

PINNING

SYMBOL	SOT188	SOT247	DESCRIPTION
TL	1	1	treble control capacitor, left channel
n.c.	2	–	not connected
B1L	3	2	bass control capacitor, left channel
B2L	4	3	bass control capacitor, left channel
OUTS	5	4	output subwoofer or output surround sound
MAD	6	5	programmable address bit (module address)
OUTL	7	6	output, left channel
n.c.	8 to 10	–	not connected
LDL	11	7	input loudness, left channel
VIL	12	8	input volume control, left channel
EOL	13	9	output effects, left channel
CAV	14	10	automatic volume control capacitor
V_{REF}	15	11	reference voltage $0.5V_{CC}$
LIL	16	12	line input, left channel
n.c.	17	–	not connected
AVL	18	13	input automatic volume control, left channel
SOL	19	14	output selector, left channel
LOL	20	15	line output, left channel
TW	21	16	capacitor timing wideband for dbx
TS	22	17	capacitor timing spectral for dbx
CW	23	18	capacitor wideband for dbx
CS	24	19	capacitor spectral for dbx
VEO	25	20	variable emphasis out for dbx
n.c.	26	–	not connected
VEI	27	21	variable emphasis in for dbx
n.c.	28	–	not connected
CNR	29	22	capacitor noise reduction for dbx
CM	30	23	capacitor mute for SAP
CD	31	24	capacitor DC decoupling for SAP
n.c.	32	–	not connected
GND	33	–	analog ground
GND	34	–	digital ground
GND	–	25	common ground
SDA	35	26	serial data input/output
SCL	36	27	serial clock input
V_{CC}	37	28	supply voltage
COMP	38	29	input composite signal
VCAP	39	30	capacitor for electronic filtering of supply
CP1	40	31	capacitor for pilot detector
CP2	41	32	capacitor for pilot detector

SYMBOL	SOT188	SOT247	DESCRIPTION
n.c.	42	–	not connected
CPH	43	33	capacitor for phase detector
n.c.	44, 45	–	not connected
CA	46	34	capacitor for filter adjust
CER	47	35	ceramic resonator
CMO	48	36	capacitor DC decoupling mono
CSS	49	37	capacitor DC decoupling stereo/SAP
LOR	50	38	line output, right channel
SOR	51	39	output selector, right channel
AVR	52	40	input automatic volume control, right channel
n.c.	53	–	not connected
LIR	54	41	line input, right channel
PS2	55	42	capacitor 2 pseudo function
PS1	56	43	capacitor 1 pseudo function
EOR	57	44	output effects, right channel
VIR	58	45	input volume control, right channel
LDR	59	46	input loudness, right channel
n.c.	60 to 62	–	not connected
OUTR	63	47	output, right channel
n.c.	64	48	not connected
SW	65	49	filter capacitor for subwoofer
B2R	66	50	bass control capacitor, right channel
B1R	67	51	bass control capacitor, right channel
TR	68	52	treble control capacitor

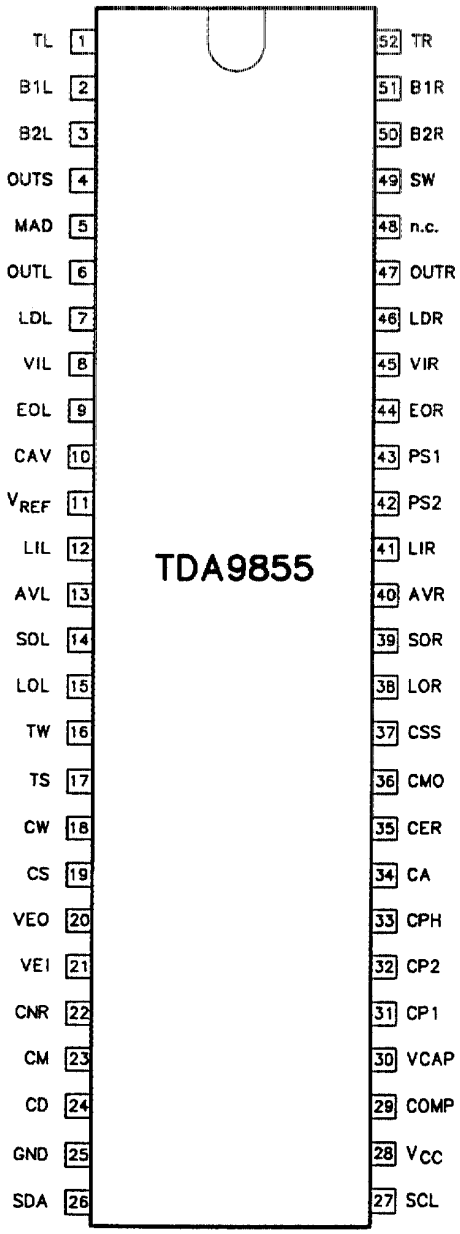


Fig.2 Pin configuration for SHRDIL-version.

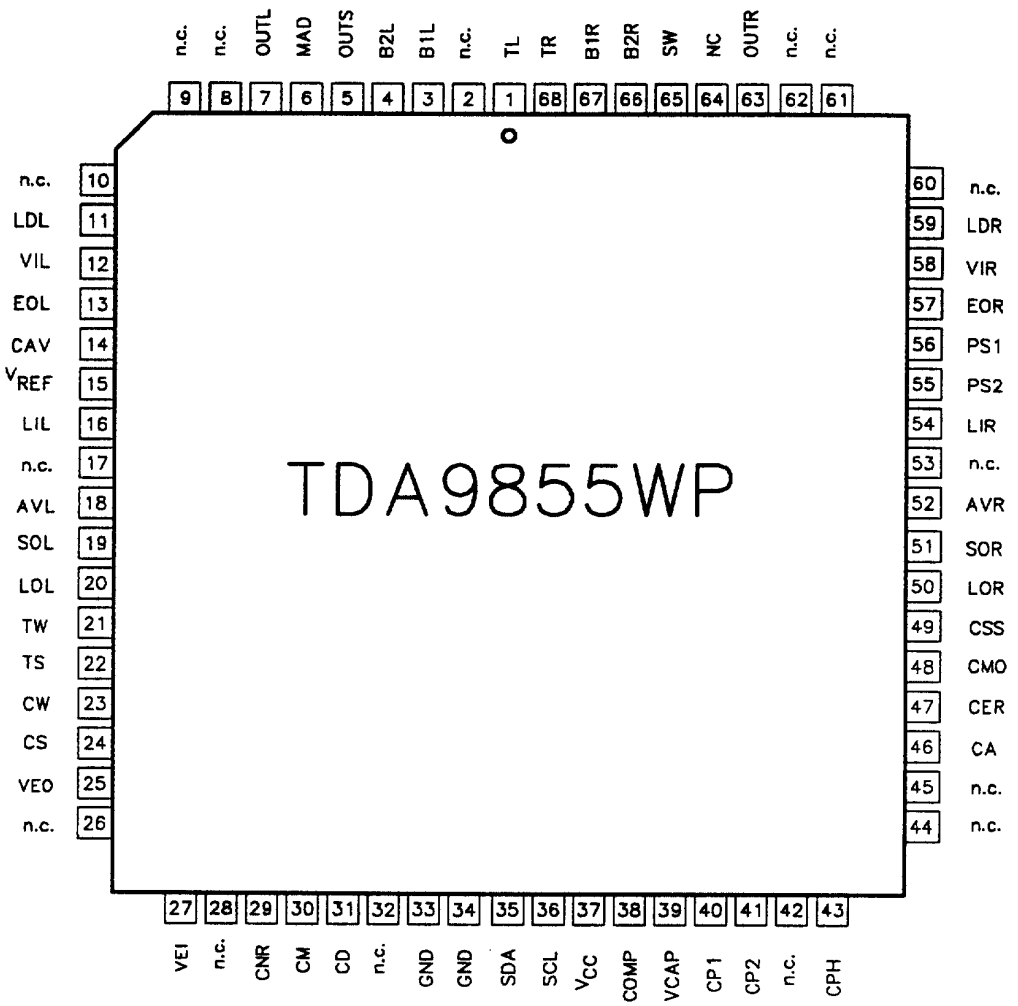


Fig.3 Pin configuration for PLCC-version.

FUNCTIONAL DESCRIPTION

Decoder

Input level adjustment

The composite input signal is fed to the input level adjustment stage. In order to compensate tolerances of the FM demodulator which supplied the composite input signal, the TDA9855 provides an input level adjustment stage. The control range is between −3.5 dB and +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 2 and 3 and the level adjust setting of Table 16 allows an optimal signal adjustment during the set alignment in the production line. This value has to be stored in a none volatile memory. The maximum input signal voltage is 2 V (RMS).

Stereo decoder

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 µs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded subsignal L − R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation can be adjusted by an automatic procedure or manually. A detailed description of this alignment is provided in the ADJUSTMENT PROCEDURE. The stereo identification can be read by the I²C-bus (see Table 1). Two different pilot thresholds can be selected via I²C-bus (see Table 18).

SAP demodulator

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in case of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 1).

Switch

The stereo/SAP switch feeds either the L − R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/line out select circuit. Table 15 shows the different switch modes provided at the output pins LOR and LOL.

dbx decoder

The dbx circuit includes all blocks required for the noise reduction system according to the BTSC system specification. The output signal is fed through a 73 µs fixed de-emphasis circuit to the dematrix block.

Integrated filters

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Audio processor

Selector

The selector allows selecting either the internal line out signals LOR or LOL (dematrix out) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Table 8). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is AC coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

Automatic volume level control

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range between 0.1 and 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched off. To avoid audible ‘plops’ during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor at pin CAV determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via I²C-bus (see notes 3 and 4 of the CHARACTERISTICS).

Effects

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono. The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via I²C-bus; see Table 13).

Volume/loudness

The volume control range is between +16 dB and −71 dB in steps of 1 dB and ends with a mute step (see Table 4). Balance control is achieved by the independent volume

control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of −12 dB. At −12 dB volume control the maximum loudness boost is obtained. The filter characteristic is determined by external components.
The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched on or off via the I²C-bus control (see Table 10). The left and right volume control stages include two independent zero crossing detectors. In the zero cross mode a change in volume is automatically activated but not executed. The execution is enabled at the next zero crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero crossing occurs the next volume transmission will enforce the last activated volume setting. The zero crossing mode is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is needed to use. In case of need to mute only one channel, two steps are necessary. The first step is a transmission from any steps to −71 dB and the second is −71 dB step to mute. The step of −71 dB to mute has no zero crossing but it is not relevant. This procedure has to be provided by software.

Bass control

A single external 33 nF capacitor for each channel in combination with a linear operational amplifier and internal resistors provides a bass control range of +16.5 dB to −12 dB in steps of 1.5 dB at low frequencies (40 Hz). Internally the basic step width is 3 dB, with intermediate steps are obtained by a toggle function that provides additional an 1.5 dB boost or attenuation (see Table 5). Please note that both loudness and bass control together result in a maximum bass boost of 34.5 dB for low volume steps.

Treble control

The adjustable range of the treble control stage is between −12 dB and +12 B in steps of 3 dB. The filter characteristic is determined by an external 5.6 nF capacitor for each channel. The logic circuitry is arranged in a way that the same data words (HEX 06 to 16) can be used for both tone controls if a bass control range from −12 dB to +12 dB and a treble control range from −12 dB to +12 dB with 3 dB steps are used (see Tables 5 and 6).

Subwoofer; surround sound control

The subwoofer or the surround mode can be activated with the control bit SUR (see Table 3). A low bit provides an output signal (L + R)/2 in subwoofer mode, a high bit selects surround mode and provides an output signal (L − R)/2. The signal is fed through a volume control stage with a range between +14 dB and −14 dB in 2 dB steps on top of the main channel control to the output pin OUTS. The last setting is the mute position (see Table 7). The capacitor C35 at pin SW provides a 230 Hz low-pass filter in subwoofer mode. In surround mode this capacitor should be disconnected. If balance is not in mid position the selected left and right output levels will be combined.

Mute

The mute function can be activated independently with the last step of volume or subwoofer/surround control at the left, right or centre output. By setting the general mute bit GMU via the I²C-bus all audio part outputs are muted. All channels include an independent zero cross detector. The zero crossing mute feature can be selected via bit TZCM:
TZCM 0:
forced mute with direct execution,
TZCM = 1:
execution in time with signal zero crossing.
In the zero cross mode a change of the GMU bit is activated but not executed. The execution is enabled at the next zero crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I²C-bus transmissions are needed:

- a first transmission for mute execution
- a second transmission about 100 ms later, which must switch the zero crossing mode to forced mute (TZCM = 0)
- a third transmission to reactivate the zero crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	9.5	V
T_{amb}	operating ambient temperature		−20	+70	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 1			
V_n	voltage at all other pins to pin GND		0	V_{CC}	V

Note to the limiting values

1. Human body model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT247AH	43 K/W
	SOT188CG	38 K/W

Requirements for the composite input signal to ensure proper system performance.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R}$	composite input level for 100% modulation L + R (25 kHz deviation), RMS, f = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = –20 to +70 °C; aging; power supply influence	–0.5	–	+0.5	dB
Z_O	output impedance	note 1	–	low-ohmic	5	kΩ
$f_{-2\ dB}$	roll-off frequencies (25 kHz deviation L + R)	low frequency (–2 dB)	–	–	5	Hz
		high frequency (–2 dB)	100	–	–	kHz
THD	total harmonic distortion L + R; f = 1 kHz	25 kHz deviation	–	–	0.5	%
		125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f = 1 kHz; 75 μs de-emphasis				
		critical picture modulation	44	–	–	dB
		with sync only	54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n x f_H; no de-emphasis; L + R: 25 kHz deviation, f = 1 kHz	40	–	–	dB

Notes to the requirements

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see input level adjustment control) must be taken into account.
2. In order to prevent clipping at overmodulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 8.5 V, source resistance ≤ 600 Ω, output load R_L ≥ 10 kΩ, C_L ≤ 2.5 nf, AC coupled; f = 1 kHz; T_{amb} = +25 °C; volume gain control G_c = 0 dB; bass linear; treble linear; loudness off; AVL off; effects linear; composite input signal according to BTSC standard; see block diagram unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current		50	75	95	mA
V_{DC}	DC voltage at signal handling pins		–	$V_{CC}/2$	–	V
DECODER SECTION						
Input level adjustment control						
G_{LA}	input level adjustment control	maximum gain	–	4.0	–	dB
		maximum attenuation	–	–3.5	–	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(RMS)}$	maximum input level		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
MPX_{L+R}	input level for 100% modulation L + R (25 kHz deviation) (RMS value)	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	–	250	–	mV
MPX_{L-R}	input level for 100% modulation L – R (50 kHz deviation) (peak value)		–	707	–	mV
MPX_{max}	headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15% for 75 μs equivalent input modulation	9	–	–	dB
MPX_{pilot}	nominal stereo pilot level (RMS value)		–	50	–	mV
ST_{ON}	pilot threshold STEREO ON (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
ST_{OFF}	pilot threshold STEREO OFF (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hyst	hysteresis		–	2.5	–	dB
Out_{L+R}	output level for 100% modulation L + R at LINE OUT	input level adjusted via I²C-bus (L + R; f = 300 Hz); monitoring LINE OUT	480	500	520	mV
α_{ST}	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation; alignment at f_L = 300 Hz; f_R = 3.1 kHz				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$L, R_{(f)}$	L, R frequency response	14% modulation; $f_{reference}$ = 300 Hz L or R				
		50 Hz to 11 kHz	–3	–	–	dB
		12 kHz	–	–3	–	dB
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; f = 1 kHz	–	0.2	1.0	%
S/N	S/N CCIR 468-2 weighted; quasi peak; V_O = 500 mV (RMS)	LINE OUT in position MONO	50	60	–	dB
Stereo decoder, oscillator (VCXO)						
f_o	nominal VCXO frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free running frequency		500.0	–	507.0	kHz
Remark: The oscillator is designed to work together with MURATA resonator CSB503F58 for TDA9855. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58 for TDA9855.						
Δf_H	capture range (nominal pilot)		±190	±265	–	Hz
SAP demodulator						
Remark: The internal SAP carrier level is determined by the composite input level and the level adjust gain.						
SAP_{IN}	nominal SAP carrier input level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
SAP_{ON}	pilot threshold SAP ON (RMS value)		–	–	85	mV
SAP_{OFF}	pilot threshold SAP OFF (RMS value)		35	–	–	mV
SAP_{HYS}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output level at LINE OUT (RMS value)	LINE OUT (LOL, LOR) in position SAP / SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
F_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; $f_{reference}$ = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	1 kHz	–	0.5	2.0	%
LINE OUT (at pins LOL, LOR)						
V_o	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
Headr	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
Out_{DC}	DC output voltage		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
R_L	output load resistance (AC)		5	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_L	output load capacitance		–	–	2.5	nF
α_{ST-SAP}	idle crosstalk L, R into SAP	100% modulation; f = 1 kHz; L or R; LINE OUT switched to SAP / SAP	50	–	–	dB
α_{SAP-ST}	idle crosstalk SAP into L, R	100% modulation; f = 1 kHz; SAP; LINE OUT switched to stereo	50	–	–	dB
ΔV_{ST-SAP}	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB
dbx noise reduction circuit						
t_{adj}	stereo adjust time	see adjustment procedure	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin 17 (pin 22) via current meter connected to $V_{CC}/2 + 1$ V	–	24	–	µA
ΔI_s	spread of timing current		–	–	15	%
$I_{s\ range}$	timing current adjustment range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$I_s/3$	–	µA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
	wideband		–	125	–	dB/s
	spectral		–	381	–	dB/s
AUDIO PART						
Circuit section from pins LIL, LIR to pins OUTL, OUTR, OUTS Select in to input line control						
B	roll-off frequencies	C_6, C_7, C_{10}, C_{26}, C_{27}, C_{29} = 2.2 µF; $Z_i = Z_{i\ min}$				
		low frequency (–3 dB)	–	–	20	Hz
		high frequency (–0.5 dB)	20	–	–	kHz
THD	total harmonic distortion	V_i = 1 V (RMS); G_c = 0 dB; AVL on	–	0.2	0.5	%
		V_i = 2 V (RMS); G_c = 0 dB; AVL on	–	0.2	0.5	%
		V_i = 1 V (RMS); G_c = 0 dB; AVL off	–	0.05	–	%
		V_i = 2 V (RMS); G_c = 0 dB; AVL off	–	0.02	–	%
RR	power supply ripple rejection	$V_{r(RMS)} < 200$ mV; f = 100 Hz	47	50	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_B	crosstalk (20 log $V_{bus(p-p)}$ / $V_{o(RMS)}$ between bus inputs and signal outputs	note 1	–	110	–	dB
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak	–	40	80	μV
		measured in dBA	–	8	–	μV
α_{CS}	channel separation	V_i = 1 V; f = 1 kHz	75	–	–	dB
		V_i = 1 V; f = 12.5 kHz	75	–	–	dB
Selector (from pins LOL, LOR, LIL, LIR to pins SOL, SOR)						
Z_i	input impedance		16	20	24	kΩ
α_S	input isolation of one selected source to the other input	f = 1 kHz; V_i = 1 V	86	96	–	dB
		f = 12.5 kHz; V_i = 1 V	80	96	–	dB
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2	2.3	–	V
$V_{DC\ OFF}$	DC offset voltage at selector out by selection of any inputs		–	–	25	mV
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
G_c	voltage gain, selector		–	0	–	dB
Automatic volume level control (AVL)						
Z_i	input impedance		8.8	11.0	13.2	kΩ
$V_{i(RMS)}$	maximum input voltage	THD < 0.2%	2	–	–	V
G_v	gain, maximum boost		5	6	7	dB
	maximum attenuation		14	15	16	dB
G_{step}	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
$V_{i(RMS)}$	input level at maximum boost	see Fig.4	–	0.1	–	V
	input level at maximum attenuation		–	1.125	–	V
$V_{o(RMS)}$	output level in AVL operation range		160	200	250	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DC\ OFF}$	DC offset between different gain steps	note 2; voltage at pin CAV				
		6.50 V to 6.33 V	–	–	6	mV
		6.33 V to 6.11 V	–	–	6	mV
		6.11 V to 5.33 V	–	–	6	mV
		5.33 V to 2.60 V	–	–	6	mV
R_{att}	discharge resistors for attack time constant	note 3;				
		AT1 = 0; AT2 = 0	340	420	520	Ω
		AT1 = 1; AT2 = 0	590	730	910	Ω
		AT1 = 0; AT2 = 1	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1	1.7	2.1	2.6	kΩ
I_{dec}	charge current for decay time	note 4	1.6	2.0	2.4	μA
Effect controls						
α_{spat1}	anti-phase crosstalk by spatial effect		–	52	–	%
α_{spat2}			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.5	–	–	–	–
Volume tone control part (input pins VIL, VIR to pins OUTX, to pin OUTS)						
Z_i	input impedance volume input		8.0	10.0	12.0	kΩ
Z_o	output impedance		–	80	120	Ω
R_L	output load resistance (AC)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$V_{i(RMS)}$	maximum input voltage	THD < 0.5%	2.0	2.15	–	V
V_{no}	noise output voltage	CCIR 468-2 weighted; quasi peak				
		G_c = 16 dB	–	110	220	μV
		G_c = 0 dB	–	33	50	μV
		mute position	–	10	–	μV
G_c	total continuous control range					
	maximum boost		–	16	–	dB
	maximum attenuation		–	71	–	dB
G_{step}	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_a	attenuation set error	G_c = +16 to –50 dB	–	–	2	dB
		G_c = –51 to –71 dB	–	–	3	dB
ΔG_t	gain tracking error	G_c = +16 to –50 dB	–	–	2	dB
α_m	mute attenuation		80	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_c = +16 to 0 dB	–	0.2	10.0	mV
		G_c = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G_c = +16 to +1 dB	–	2	15	mV
		G_c = 0 to –71 dB	–	1	10	mV
Loudness control part						
L_B	maximum loudness boost	loudness on; referred to loudness off; boost is determined by external components; see Fig.6;				
		f = 40 Hz	–	17	–	dB
		f = 10 kHz	–	4.5	–	dB
Bass control (see Fig.7)						
G_b	bass control maximum boost	f = 40 Hz	15.5	16.5	17.5	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
G_{step}	step resolution	f = 40 Hz	–	1.5	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	15	mV
Treble control (see Fig.8)						
G_t	treble control maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
	maximum boost	f > 15 kHz	–	–	15	dB
G_{step}	step resolution	f = 15 kHz	–	3	–	dB
	step error between any adjoining step		–	–	0.5	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step		–	–	10	mV
Subwoofer or surround control						
G_s	subwoofer control	f = 40 Hz				
	maximum boost		12	14	16	dB
	maximum attenuation		12	14	16	dB
G_{step}	step resolution		–	2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_m	mute attenuation		60	–	–	dB
$V_{DC\ OFF}$	DC step offset between any adjacent step	G_S = 0 to +14 dB	–	–	10	mV
		G_S = 0 to –14 dB	–	–	5	mV
	DC step offset between any step to mute	G_S = +2 to +14 dB without input offset (pin SW connected to V_{REF})	–	–	15	mV
		G_S = +2 to +14 dB inclusive offset from OUTR, OUTL	–	–	50	mV
		G_S = 0 to –14 dB	–	–	10	mV
R_F	internal resistor for low-pass filter with external capacitor at pin SW		4	5	6	kΩ
$L + R_{REJ}$	common mode rejection in surround sound at pin OUTS	mono signal at VIL/VIR; F = 1 kHz; V_i = 1 V; balance = 0 dB	26	36	–	dB
Muting at power supply drop for OUTL, OUTR, OUTS						
$V_{CC\text{-}DROP}$	supply drop for mute active		–	V_{CAP} – 0.7	–	V
Power on reset						
When reset is active the GMU-bit (general mute) and the LMU-bit (LINEOUT - mute) is set and the I²C-bus receiver is in reset position						
V_{CC}	start of reset	increasing supply voltage	–	–	2.5	V
	end of reset		5.2	6	6.8	V
	start of reset	decreasing supply voltage	4.2	5	5.8	V
Digital part (I²C-bus pins; note 5**)**						
V_{IH}	HIGH level input voltage		3	–	V_{CC}	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_L = 3 mA	–	–	0.4	V

Notes to the characteristics

1. The transmission contains:
   - total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   - clock frequency = 50 kHz
   - repetition burst rate = 400 Hz
   - maximum bus signal amplitude = 5 V_{p-p}.
2. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, −6 dB, −15 dB.
3. Attack time constant = C_{AV} x R_{att}.
4. Decay time = $$\frac{C_{AV} \times 0.76\ V \left(10^{-\frac{G_{v1}}{20}} - 10^{-\frac{G_{v2}}{20}} \right)}{I_{dec}}$$

   Example: C_{AV} = 4.7 µF; I_{dec} = 2 µA; G_{v1} = −9 dB; G_{v2} = +6 dB → decay time result: 4.14 s.
5. The AC characteristics are in accordance with the I²C-bus specification. Full specification of I²C-bus will be supplied on request. The maximum clock frequency is 100 kHz.

ADJUSTMENT PROCEDURE

Composite input level adjustment. Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R, f = 300 Hz. Set input level control via I²C-bus monitoring line out (500 mV ± 20 mV). Store the setting in a none volatile memory. Adjustment of spectral and wideband expander via stereo channel separation adjust.

Automatic adjustment procedure

- Capacitors of external inputs EIL, EIR must be grounded
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via I²C-bus. To avoid annoying sound level set GMU bit to '1' during adjustment procedure
- Effects, AVL, loudness off
- Selector setting SC0, SC1, SC2 = 0, 0, 0 (see Table 8)
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 15)
- Start adjustment by transmission ADJ = 1 in register ALI3. The decoder will align itself
- After 1 s, stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see I²C-bus protocol) and store it in a none volatile memory. The alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

Manual adjust

Manual adjust is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz, 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz, 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimal adjust
- Store data in none volatile memory.

After every POWER ON, the alignment data and the input level adjustment data must be loaded from the none volatile memory.

Timing current for release rate

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 19, as recommended by dbx.

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/W	A	DATA	MA	DATA	P

Where:

S	=	start condition, generated by the master
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	1 (read), generated by the master
A	=	acknowledge, generated by the slave
DATA	=	slave transmits an 8-bit data word
MA	=	acknowledge, generated by the master
P	=	stop condition, generated by the master

Table 1 Definition of the transmitted bytes after read condition.

FUNCTION	BYTE	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Function of the bits:

STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1x to A2x	stereo alignment read data
A1x	for wideband expander
A2x	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word, ALR1, then the slave transmits the next data word ALR2. The master next generates an acknowledge, then the slave begins transmitting the first data word ALR1, and so on until the master generates no acknowledge and transmits condition P.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/W	A	SUBADDRESS	A	DATA	A	P

Where:

S	=	start condition
standard SLAVE ADDRESS	=	101 101 1 pin MAD not connected
pin programmable SLAVE ADDRESS	=	101 101 0 pin MAD connected to ground
R/W	=	0 (write)
A	=	acknowledge, generated by the slave
SUBADDRESS (SAD)	=	see Table 2
DATA	=	see Table 3
P	=	stop condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress according to the order of Table 2 is performed.

Subaddress

Table 2 Second byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	HEX
volume right	VR	0	0	0	0	0	0	0	0	00
volume left	VL	0	0	0	0	0	0	0	1	01
bass	BA	0	0	0	0	0	0	1	0	02
treble	TR	0	0	0	0	0	0	1	1	03
subwoofer	SW	0	0	0	0	0	1	0	0	04
control 1	CON1	0	0	0	0	0	1	0	1	05
control 2	CON2	0	0	0	0	0	1	1	0	06
control 3	CON3	0	0	0	0	0	1	1	1	07
alignment 1	ALI1	0	0	0	0	1	0	0	0	08
alignment 2	ALI2	0	0	0	0	1	0	0	1	09
alignment 3	ALI3	0	0	0	0	1	0	1	0	0A

Definition of third byte

Table 3 Third byte after slave address.

FUNCTION	REGISTER	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0
volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0
bass	BA	0	0	0	BA4	BA3	BA2	BA1	BA0
treble	TR	0	0	0	TR4	TR3	TR2	TR1	0
subwoofer	SW	0	0	SW5	SW4	SW3	SW2	0	0
control 1	CON1	GMU	AVLON	LOFF	0	SUR	SC2	SC1	SC0
control 2	CON2	SAP	STEREO	TZCM	VZCM	LMU	EF2	EF1	EF0
control 3	CON3	0	0	0	0	L3	L2	L1	L0
alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
alignment 3	ALI3	ADJ	AT1	AT2	0	1	TC2	TC1	TC0

Function of the bits:

VR0 to VR6	volume control right
VL0 to VL6	volume control left
BA0 to BA4	bass control
TR1 to TR3	treble control
SW2 to SW5	subwoofer, surround control
GMU	mute control for all outputs (general mute)
AVLON	AVL on/off
LOFF	switch loudness on/off
SUR	surrounds/subwoofer SUR = 1 $\rightarrow$ (L – R)/2; SUR = 0 $\rightarrow$ (L + R)/2
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero cross mode in mute operation (treble and subwoofer/surround output stage)
VZCM	zero cross mode in volume operation
LMU	mute control for line out
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjust
ADJ	stereo adjust on/off
A1X	stereo alignment data for wideband expander
A2X	stereo alignment data for spectral expander
AT1, AT2	attack time at AVL
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 4 Volume setting in register VR and VL.

G_c (dB)	DATA D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	HEX
16	1	1	1	1	1	1	1	7F
15	1	1	1	1	1	1	0	7E
14	1	1	1	1	1	0	1	7D
13	1	1	1	1	1	0	0	7C
12	1	1	1	1	0	1	1	7B
11	1	1	1	1	0	1	0	7A
10	1	1	1	1	0	0	1	79
9	1	1	1	1	0	0	0	78
8	1	1	1	0	1	1	1	77
7	1	1	1	0	1	1	0	76
6	1	1	1	0	1	0	1	75
5	1	1	1	0	1	0	0	74
4	1	1	1	0	0	1	1	73
3	1	1	1	0	0	1	0	72
2	1	1	1	0	0	0	1	71
1	1	1	1	0	0	0	0	70
0	1	1	0	1	1	1	1	6F
–1	1	1	0	1	1	1	0	6E
–2	1	1	0	1	1	0	1	6D
–3	1	1	0	1	1	0	0	6C
–4	1	1	0	1	0	1	1	6B
–5	1	1	0	1	0	1	0	6A
–6	1	1	0	1	0	0	1	69
–7	1	1	0	1	0	0	0	68
–8	1	1	0	0	1	1	1	67
–9	1	1	0	0	1	1	0	66
–10	1	1	0	0	1	0	1	65
–11	1	1	0	0	1	0	0	64
–12	1	1	0	0	0	1	1	63
–13	1	1	0	0	0	1	0	62
–14	1	1	0	0	0	0	1	61
–15	1	1	0	0	0	0	0	60

G_c (dB)	DATA D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	HEX
–16	1	0	1	1	1	1	1	5F
–17	1	0	1	1	1	1	0	5E
–18	1	0	1	1	1	0	1	5D
–19	1	0	1	1	1	0	0	5C
–20	1	0	1	1	0	1	1	5B
–21	1	0	1	1	0	1	0	5A
–22	1	0	1	1	0	0	1	59
–23	1	0	1	1	0	0	0	58
–24	1	0	1	0	1	1	1	57
–25	1	0	1	0	1	1	0	56
–26	1	0	1	0	1	0	1	55
–27	1	0	1	0	1	0	0	54
–28	1	0	1	0	0	1	1	53
–29	1	0	1	0	0	1	0	52
–30	1	0	1	0	0	0	1	51
–31	1	0	1	0	0	0	0	50
–32	1	0	0	1	1	1	1	4F
–33	1	0	0	1	1	1	0	4E
–34	1	0	0	1	1	0	1	4D
–35	1	0	0	1	1	0	0	4C
–36	1	0	0	1	0	1	1	4B
–37	1	0	0	1	0	1	0	4A
–38	1	0	0	1	0	0	1	49
–39	1	0	0	1	0	0	0	48
–40	1	0	0	0	1	1	1	47
–41	1	0	0	0	1	1	0	46
–42	1	0	0	0	1	0	1	45
–43	1	0	0	0	1	0	0	44
–44	1	0	0	0	0	1	1	43
–45	1	0	0	0	0	1	0	42
–46	1	0	0	0	0	0	1	41
–47	1	0	0	0	0	0	0	40

G_c (dB)	DATA D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	HEX
–48	0	1	1	1	1	1	1	3F
–49	0	1	1	1	1	1	0	3E
–50	0	1	1	1	1	0	1	3D
–51	0	1	1	1	1	0	0	3C
–52	0	1	1	1	0	1	1	3B
–53	0	1	1	1	0	1	0	3A
–54	0	1	1	1	0	0	1	39
–55	0	1	1	1	0	0	0	38
–56	0	1	1	0	1	1	1	37
–57	0	1	1	0	1	1	0	36
–58	0	1	1	0	1	0	1	35
–59	0	1	1	0	1	0	0	34
–60	0	1	1	0	0	1	1	33
–61	0	1	1	0	0	1	0	32
–62	0	1	1	0	0	0	1	31
–63	0	1	1	0	0	0	0	30
–64	0	1	0	1	1	1	1	2F
–65	0	1	0	1	1	1	0	2E
–66	0	1	0	1	1	0	1	2D
–67	0	1	0	1	1	0	0	2C
–68	0	1	0	1	0	1	1	2B
–69	0	1	0	1	0	1	0	2A
–70	0	1	0	1	0	0	1	29
–71	0	1	0	1	0	0	0	28
mute	0	1	0	0	1	1	1	27

Table 5 Bass setting in register BA.

G_b (dB)	DATA D4 BA4	D3 BA3	D2 BA2	D1 BA1	D0 BA0	HEX
16.5	1	1	0	0	1	19
15	1	1	0	0	0	18
13.5	1	0	1	1	1	17
12	1	0	1	1	0	16
10.5	1	0	1	0	1	15
9	1	0	1	0	0	14
7.5	1	0	0	1	1	13
6	1	0	0	1	0	12
4.5	1	0	0	0	1	11
3	1	0	0	0	0	10
1.5	0	1	1	1	1	0F
0	0	1	1	1	0	0E
–1.5	0	1	1	0	1	0D
–3	0	1	1	0	0	0C
–4.5	0	1	0	1	1	0B
–6	0	1	0	1	0	0A
–7.5	0	1	0	0	1	09
–9	0	1	0	0	0	08
–10.5	0	0	1	1	1	07
–12	0	0	1	1	0	06

Table 6 Treble setting in register TR.

G_t (dB)	DATA D4 TR4	D3 TR3	D2 TR2	D1 TR1	HEX
12	1	0	1	1	16
9	1	0	1	0	14
6	1	0	0	1	12
3	1	0	0	0	10
0	0	1	1	1	0E
–3	0	1	1	0	0C
–6	0	1	0	1	0A
–9	0	1	0	0	08
–12	0	0	1	1	06

Table 7 Subwoofer/surround setting in register SW.

G_s(dB)	DATA D5 SW5	D4 SW4	D3 SW3	D2 SW2	HEX
14	1	1	1	1	3C
12	1	1	1	0	38
10	1	1	0	1	34
8	1	1	0	0	30
6	1	0	1	1	2C
4	1	0	1	0	28
2	1	0	0	1	24
0	1	0	0	0	20
–2	0	1	1	1	1C
–4	0	1	1	0	18
–6	0	1	0	1	14
–8	0	1	0	0	10
–10	0	0	1	1	0C
–12	0	0	1	0	08
–14	0	0	0	1	04
mute	0	0	0	0	00

Table 8 Selector setting in register CON1.

FUNCTION: input connected to		DATA D2 SC2	D1 SC1	D0 SC0
output	SOR, SOL			
input	LOR, LOL	0	0	0
input	LOR, LOR	0	0	1
input	LOL, LOL	0	1	0
input	LOL, LOR	0	1	1
input	LIR, LIL	1	0	0
input	LIR, LIR	1	0	1
input	LIL, LIL	1	1	0
input	LIL, LIR	1	1	1

Table 9 SUR bit setting in register CON1.

FUNCTION	DATA D3
surround sound	1
subwoofer	0

Table 10 LOFF bit setting in register CON1.

CHARACTERISTIC	DATA D5
with loudness	0
linear	1

Table 11 AVLON bit setting in register CON1.

FUNCTION	DATA D6
automatic volume control off	0
automatic volume control on	1

Table 12 Mute setting.

REGISTER CON1		REGISTER CON2	
FUNCTION	DATA D7 GMU	FUNCTION	DATA D3 LMU
forced mute at OUTR, OUTL, OUTS	1	forced mute at LOR, LOL	1
audio processor controlled outputs	0	stereo processor controlled outputs	0

Table 13 Effects setting in register CON2.

FUNCTION	DATA D2 EF2	D1 EF1	D0 EF0
stereo linear on	0	0	0
pseudo on	0	0	1
spatial stereo, 30% anti-phase crosstalk	0	1	0
spatial stereo, 50% anti-phase crosstalk	0	1	1
forced mono	1	1	1

Table 14 Zero cross detection setting in register CON2.

FUNCTION	DATA D5 TZCM	FUNCTION	DATA D4 VZCM
direct mute control	0	direct volume control	0
mute control delayed until the next zero crossing	1	volume control delayed until the next zero crossing	1

Table 15 Switch setting at line out.

FUNCTION		DATA	DATA	
line out signals at		**transmission status**	**setting bits in register CON2**	
LOL	**LOR**	**internal switch readable bits in register ALR1, ALR2:** **D6 SAPP** **D5 STP**	**D7 SAP**	**D6 STEREO**
SAP	SAP	SAP received	1	1
mute	mute	no SAP received	1	1
left	right	stereo received	0	1
mono	mono	no stereo received	0	1
mono	SAP	SAP received	1	0
mono	mute	no SAP received	1	0
mono	mono		0	0

Table 16 Level adjust setting in register CON3.

G_I (dB)	DATA D3 L3	D2 L2	D1 L1	D0 L0	HEX
+4	1	1	1	1	0F
+3.5	1	1	1	0	0E
+3	1	1	0	1	0D
+2.5	1	1	0	0	0C
+2	1	0	1	1	0B
+1.5	1	0	1	0	0A
+1	1	0	0	1	09
+0.5	1	0	0	0	08
0	0	1	1	1	07
−0.5	0	1	1	0	06
−1	0	1	0	1	05
−1.5	0	1	0	0	04
−2	0	0	1	1	03
−2.5	0	0	1	0	02
−3	0	0	0	1	01
−3.5	0	0	0	0	00

Table 17 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2.

FUNCTION	DATA				
	D4 AX4	D3 AX3	D2 AX2	D1 AX1	D0 AX0
gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
nominal gain	1	0	0	0	0
	0	1	1	1	1
gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0

Table 18 STS bit setting in register ALI2 (pilot threshold stereo on).

FUNCTION	DATA D7
STON ≤ 35 mV	1
STON ≤ 30 mV	0

Table 19 Timing current setting in register ALI3.

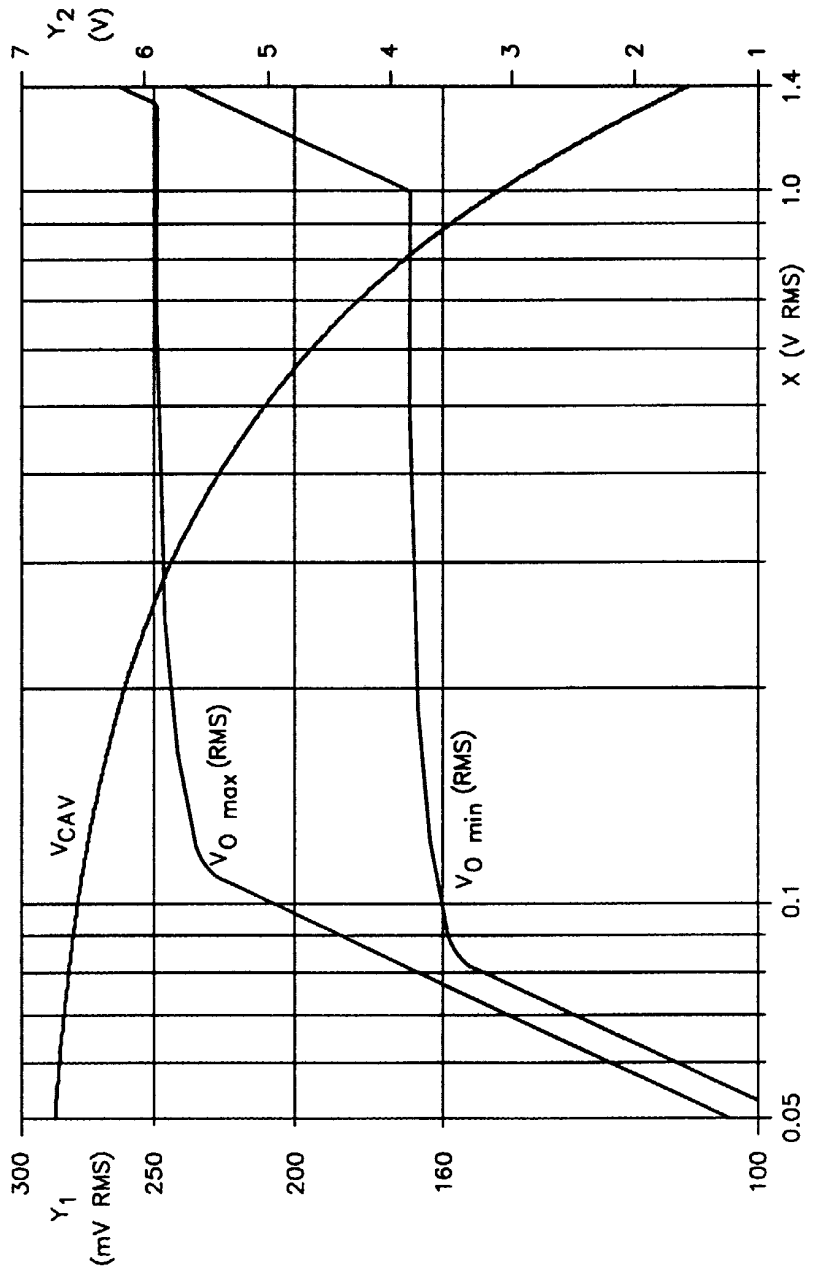
$I_{s\ range}$	DATA		
	D2 TC2	D1 TC1	D0 TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	0
nominal	0	1	1
–10%	0	1	0
–20%	0	0	1
–30%	0	0	0

Table 20 AVL attack time setting in register ALI3.

R_{att} (Ω)	DATA	
	D6 AT1	D5 AT2
420	0	0
730	1	0
1200	0	1
2100	1	1

Table 21 ADJ bit setting in register ALI3.

FUNCTION	DATA D7
stereo decoder operation mode	0
auto adjustment of channel separation	1



AVL measured at pin EOL/EOR
Y_1 axis: output level in AVL operation with typically 200 mV
Y_2 axis: V_{CAV} DC voltage at pin CAV corresponds with typically gain steps in a range of +6 to −15 dB
X axis: input level V_i

Fig.4 Automatic volume level control diagram.

CURVE	CAPACITANCE AT PIN 43 (56) (nF)	CAPACITANCE AT PIN 42 (55) (nF)	EFFECT
1	15	15	normal
2	5.6	47	intensified
3	5.6	68	more intensified

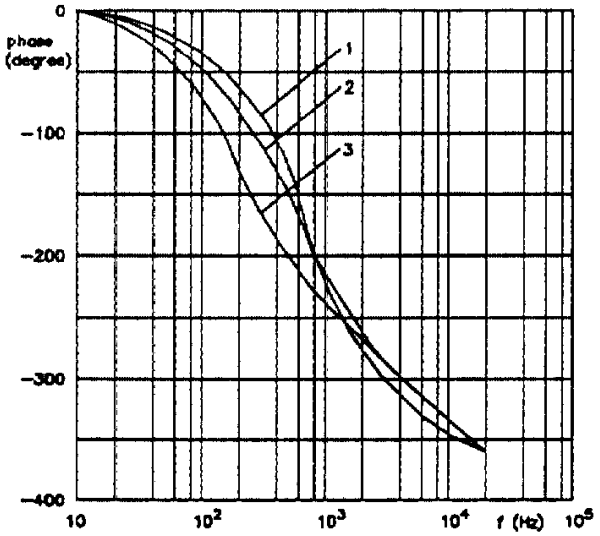


Fig.5 Pseudo (phase in degrees) as a function of frequency (left output).

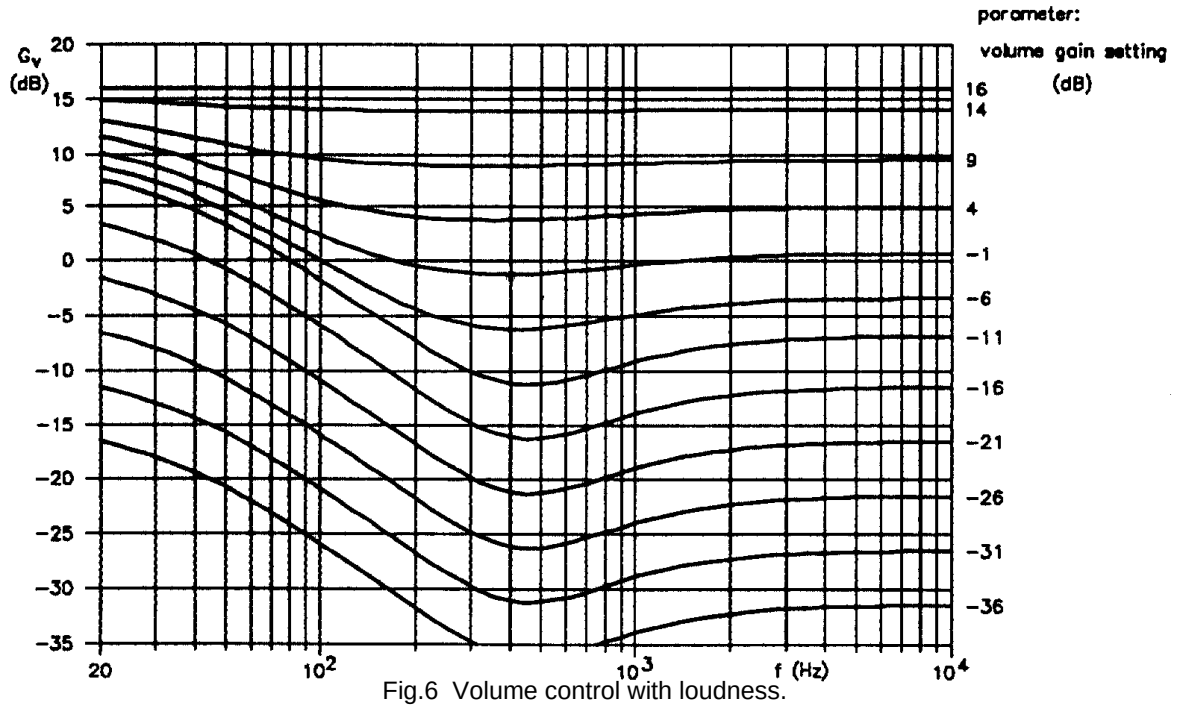


Fig.6 Volume control with loudness.

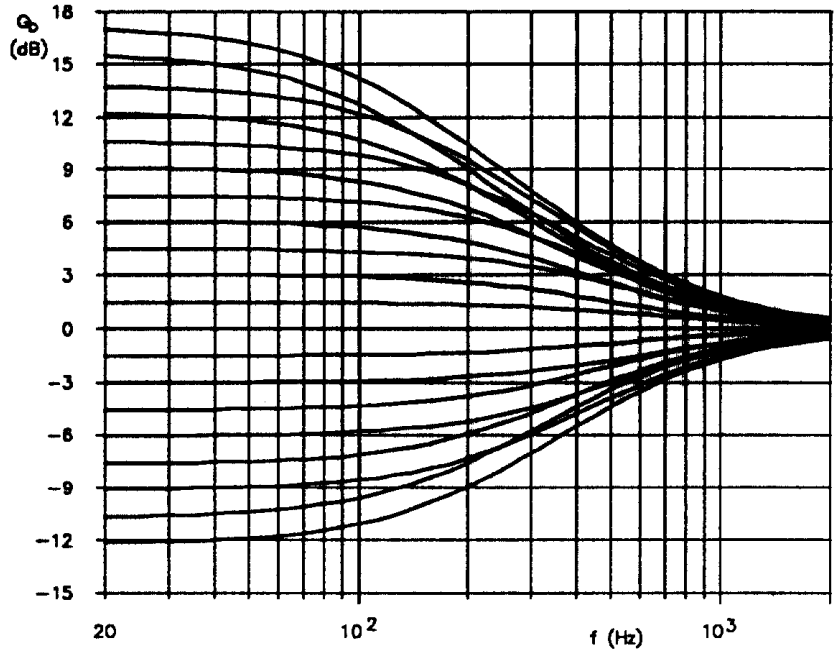


Fig.7 Bass control.

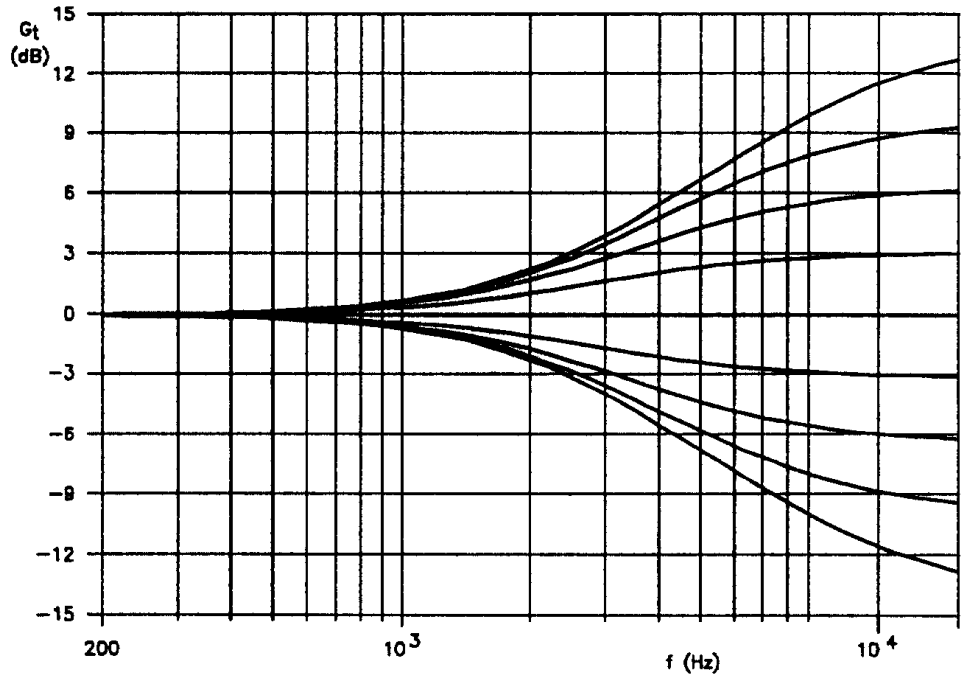


Fig.8 Treble control.

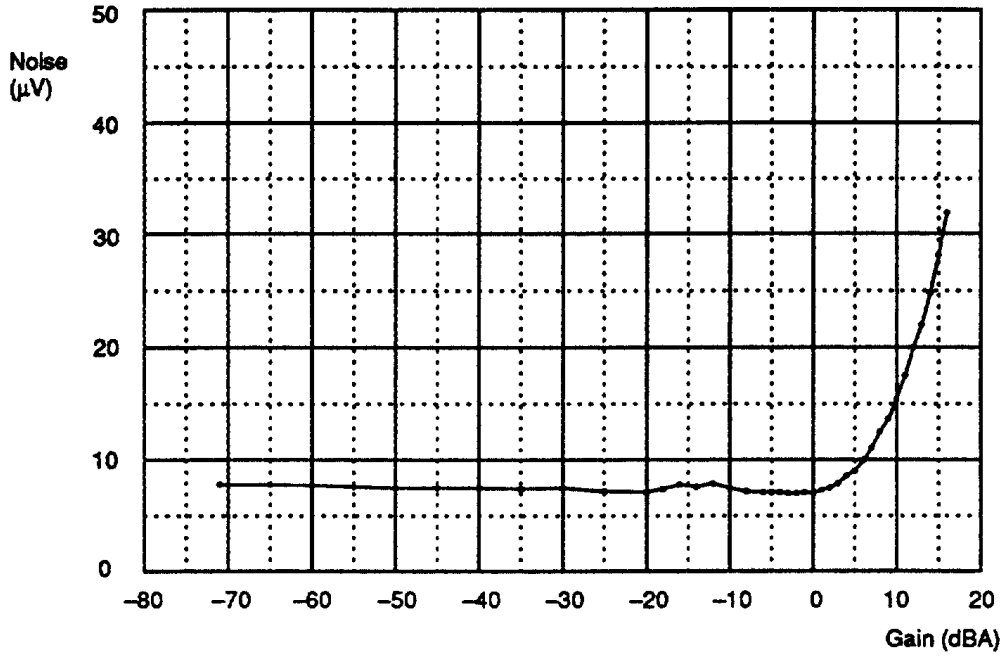


Fig.9 Noise as function of gain in dBA (RMS value).

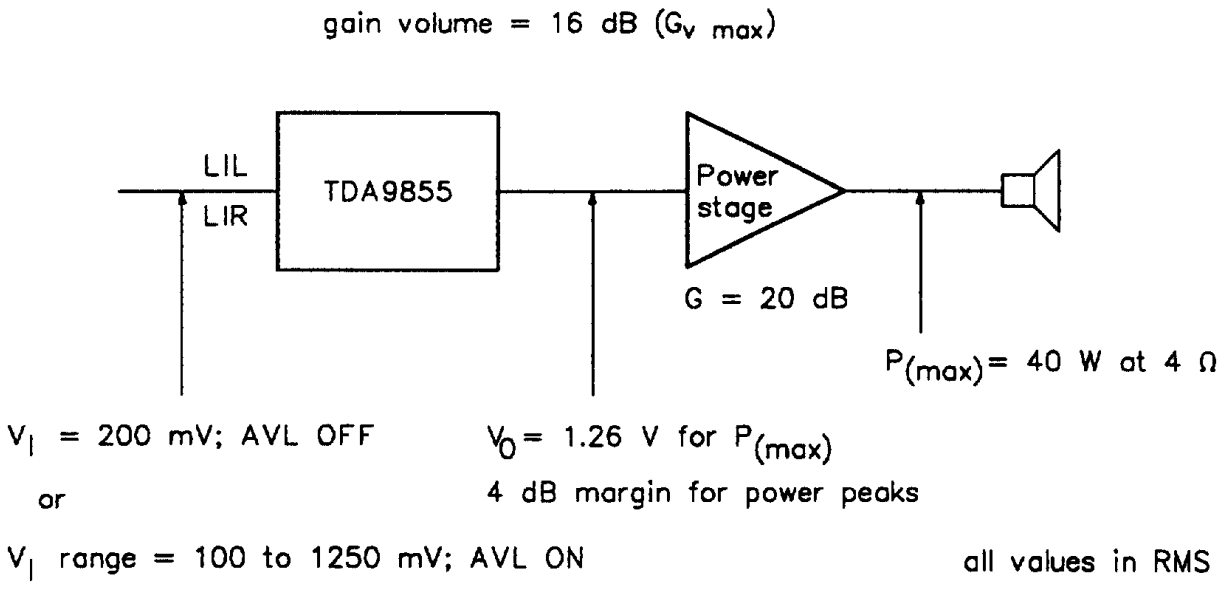


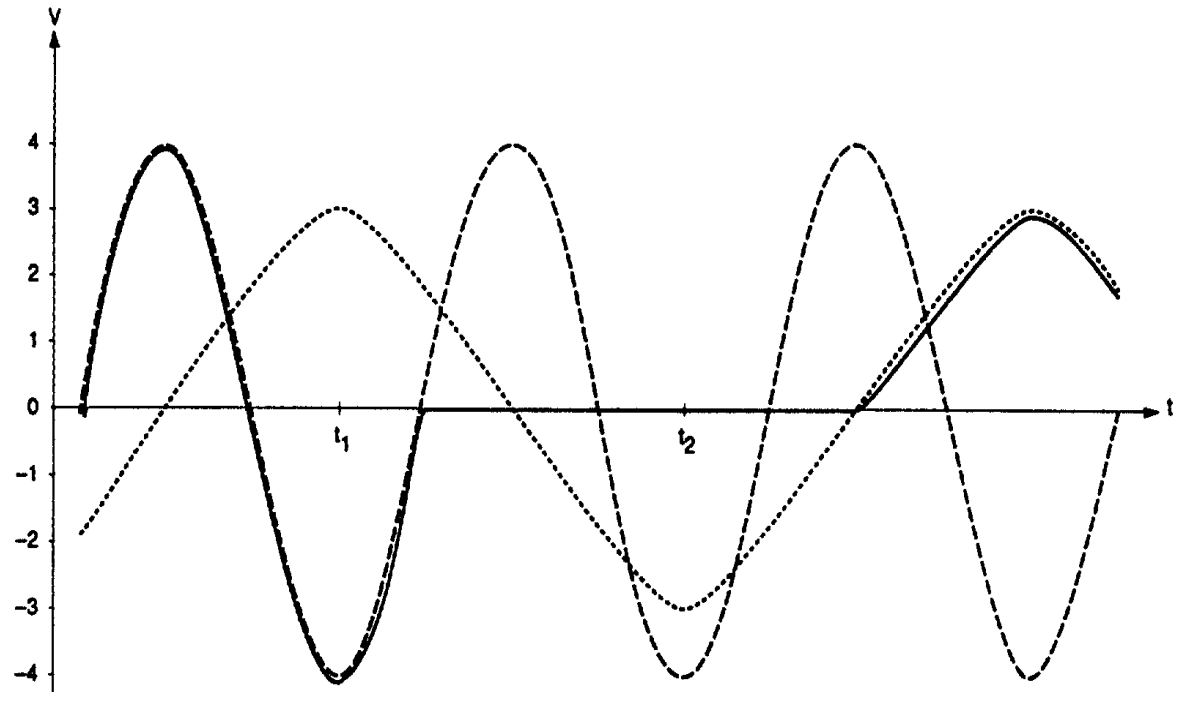
Fig.10 Level diagram.

APPLICATION HINTS

Selection of input signals by using the zero crossing mute mode

A selection between the internal signal path and the external input LIL/LIR produces a modulation click depending on the difference of the signal values at the time of switching. At t_1 the maximum possible difference between signals is 7 $V_{(p-p)}$ and gives a large click. Using the zero cross detector no modulation click is audible. For example: The selection is enabled at t_1, the microcontroller sets the zero cross bit (TZCM = 1) and then the mute bit (GMU = 1) via the I²C-bus. The output signal follows the input A signal, until the next zero crossing occurs and then activates mute.
After a fixed delay time before t_2, the microcontroller has to send the forced mute mode (TZCM = 0) and the return to the zero crossing mode (TZCM = 1) to be sure that mute is enabled.

The output signal remains muted until the next signal zero crossing of input B occurs, and then follows that signal. The delay time $t_2 - t_1$ is e.g. 40 ms. The zero cross function is working at the lowest frequency of 40 Hz.



——— output
- - - input B (external input signal)
— — input A (internal signal)

Fig.11 Zero cross function; only one channel shown.

Loudness filter calculation example

Fig.12 shows the basic loudness circuit with an external low-pass filter application. R_1 allows an attenuation range of
21 dB while the boost is determined by the gain stage V_1. Both result in a loudness control range of +16 dB to –12 dB.
Defining $f_{reference}$ as the frequency where the level does not change while switching loudness on/off. The external resistor R_3 for $f_{reference} \rightarrow \infty$ can be calculated as

$$R_3 = R_1 \frac{10^{G_v/20}}{1 - 10^{G_v/20}}$$

with G_v = –21 dB and R_1 = 33 kΩ results in R_3 = 3.2 kΩ.
For the low-pass filter characteristic the value of the external capacitor C_1 can be determined by setting a specific boost for a defined frequency and referring the gain to G_v at $f_{reference}$ as indicated above.

$$\left|\frac{1}{j\omega C_1}\right| = \frac{(R_1 + R_3) \times 10^{G_v/20} - R_3}{1 - 10^{G_v/20}}$$

For example: 3 dB boost at f = 1 kHz $G_v = G_{v\,reference}$ + 3 dB = –18 dB; f = 1 kHz and C_1 = 100 nF
If a loudness characteristic with additional high frequency boost is desired, an additional high-pass section has to be included in the external filter circuit as indicated in the block diagram. A filter configuration that provides AC coupling avoids offset voltage problems.
Fig.13 shows an example of the loudness circuit with bass and treble boost.

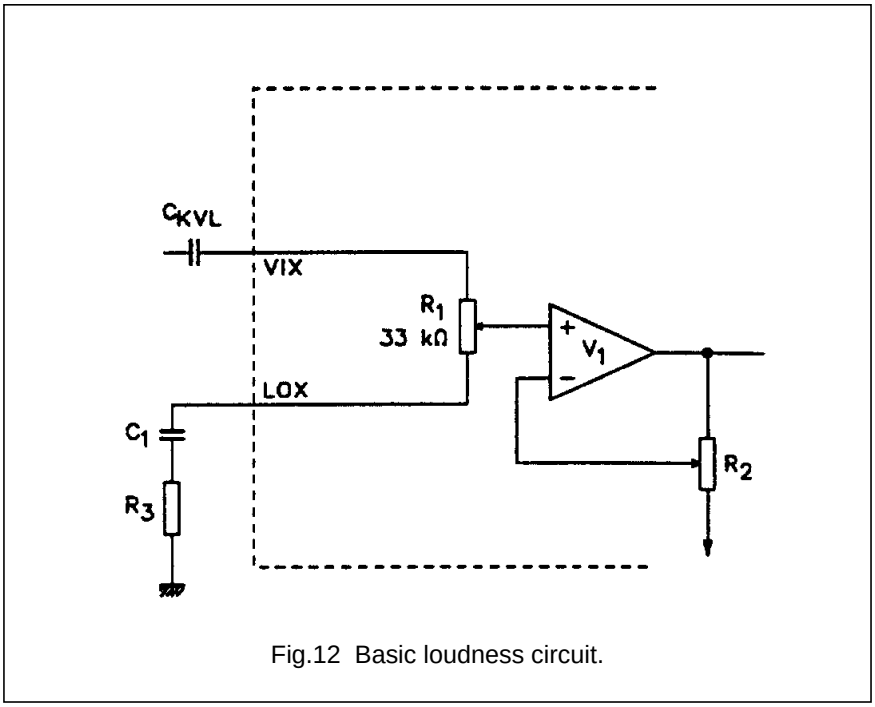


Fig.12 Basic loudness circuit.

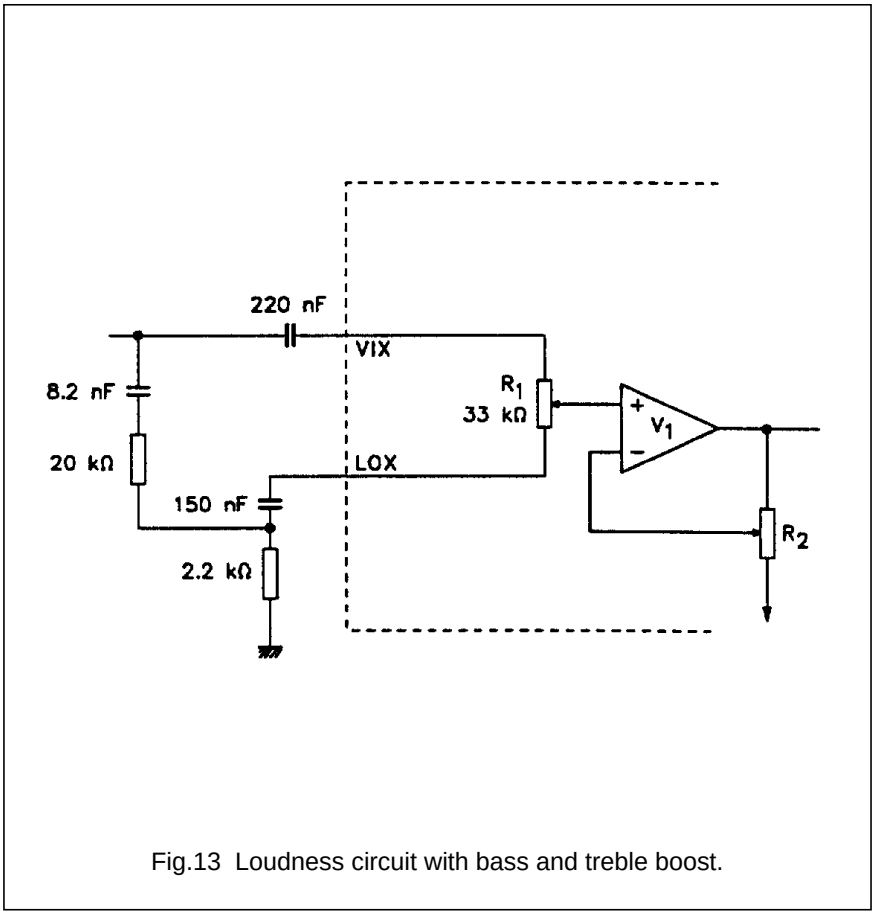


Fig.13 Loudness circuit with bass and treble boost.

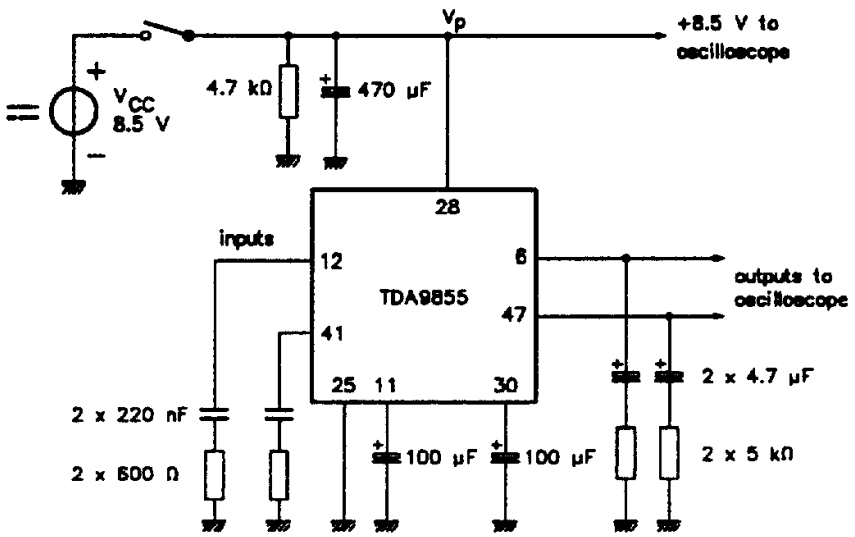


Fig.14 Turn-on/off power supply circuit diagram.

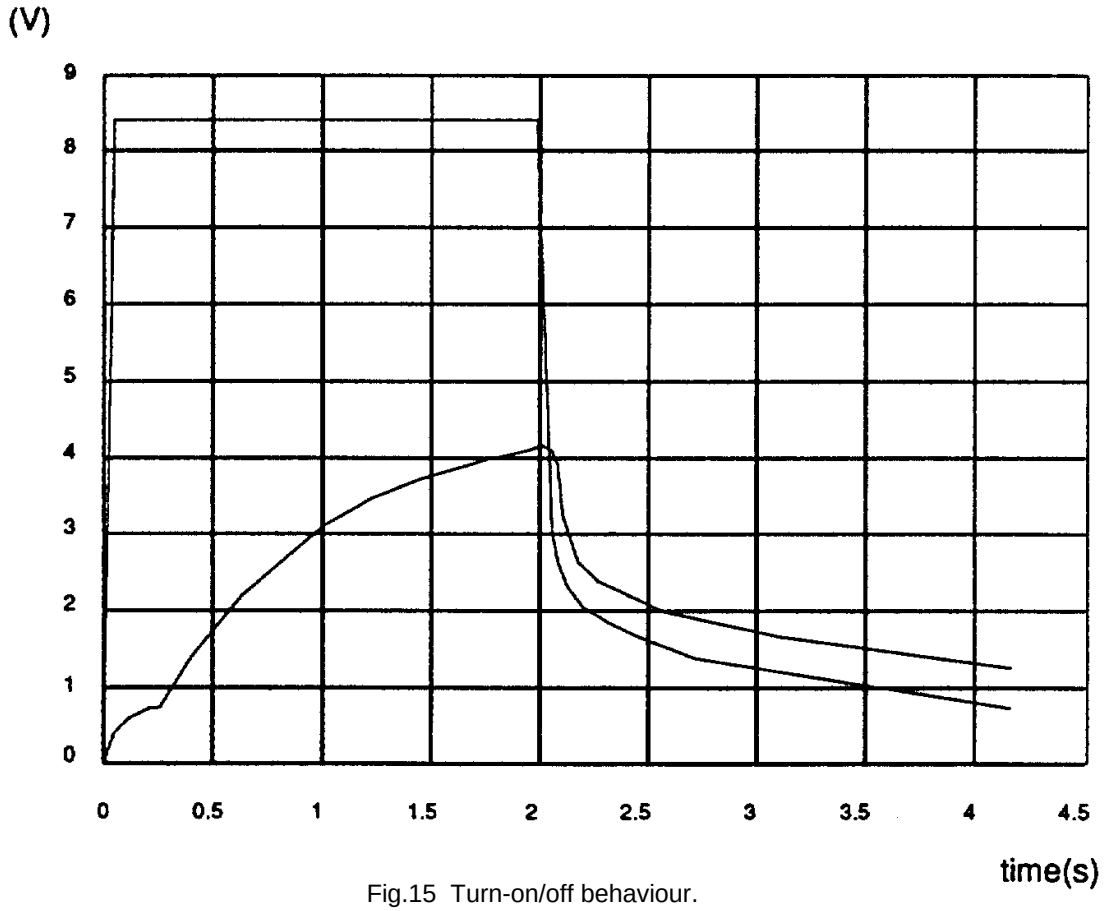
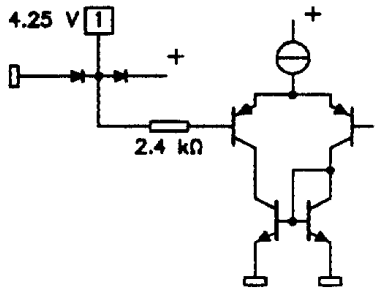
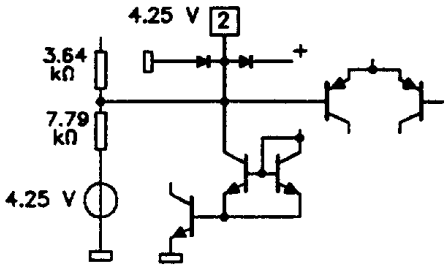


Fig.15 Turn-on/off behaviour.

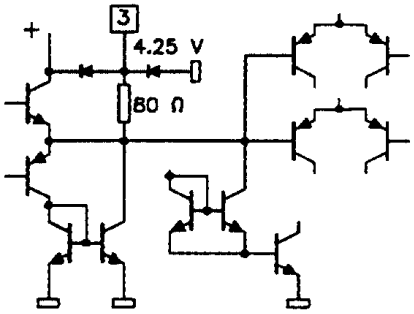
INTERNAL PIN CONFIGURATIONS (pin numbers for SHRDIL-version)



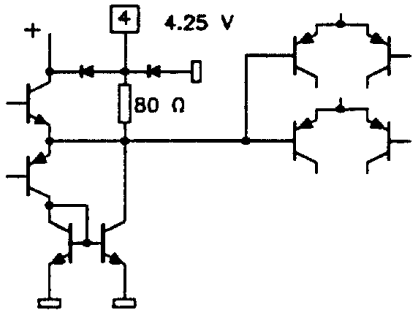
Pin 1: Treble control capacitor, left
Pin 52: Treble control capacitor, right



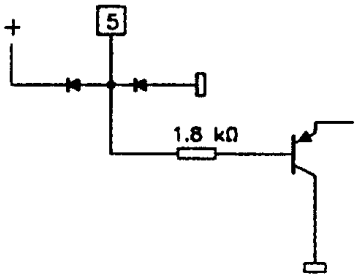
Pin 2: Bass control capacitor input, left
Pin 51: Bass control capacitor input, right



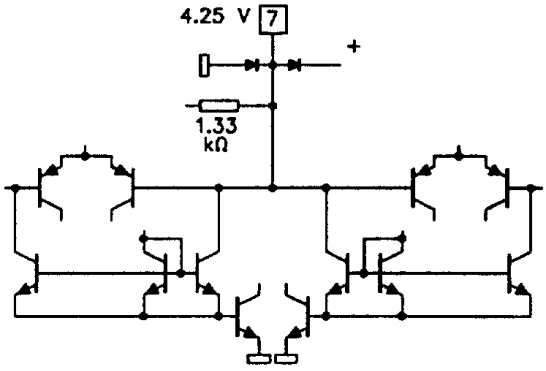
Pin 3: Bass control capacitor output, left
Pin 50: Bass control capacitor output, right



Pin 4: Output subwoofer
Pin 6: Output, left channel
Pin 14: Output selector, left channel
Pin 39: Output selector, right channel
Pin 47: Output, right channel

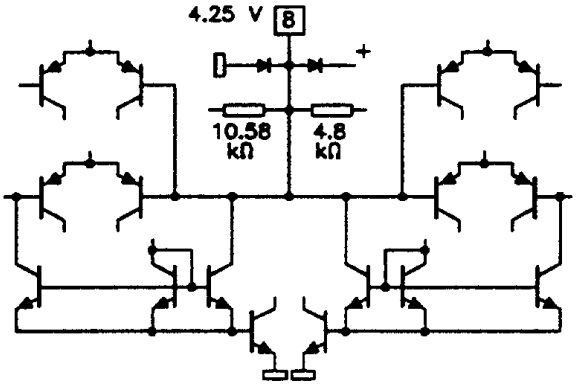


Pin 5: MAD (I²C-bus address switch)

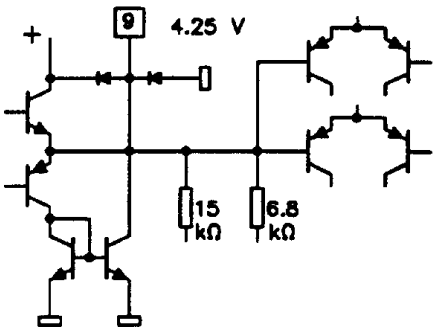


Pin 7: Input loudnes, left
Pin 46: Input loudness, right

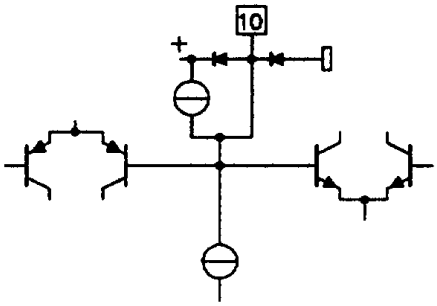
Fig.16 Internal circuits (continued in Fig.17).



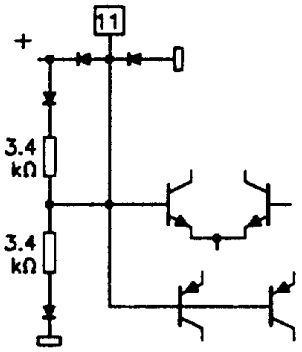
Pin 8: Input volume, left
Pin 45: Input volume, right



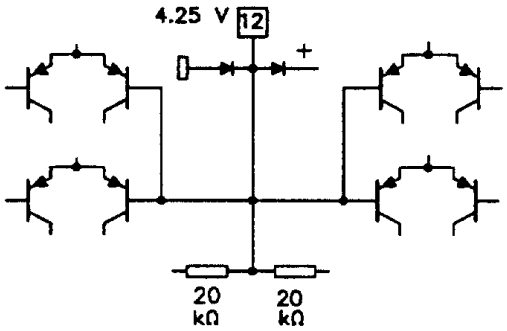
Pin 9: Output effects, left
Pin 44: Output effects, right



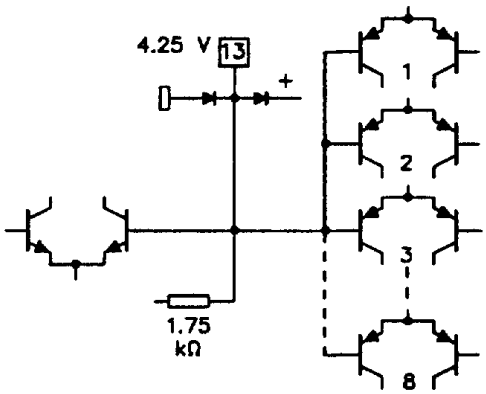
Pin 10: Automatic volume control capacitor



Pin 11: Reference voltage
$0.5 \times V_{CC}$

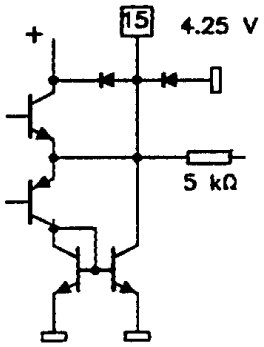


Pin 12: Line input, left
Pin 41: Line input, right

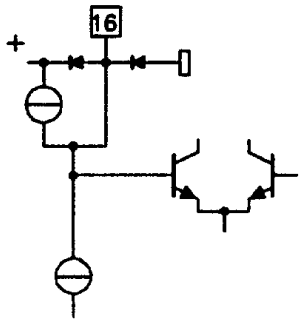


Pin 13: Input automatic volume control, left
Pin 40: Input automatic volume control, right

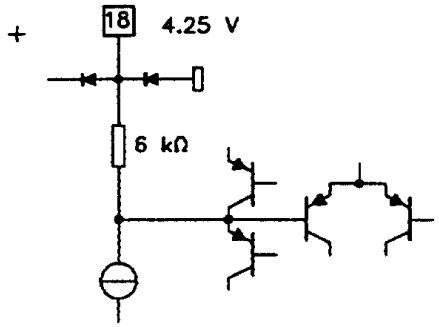
Fig.17 Internal circuits (continued from Fig.16).



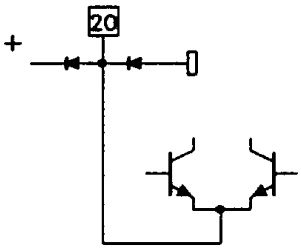
Pin 15: Line output, left
Pin 38: Line output, right



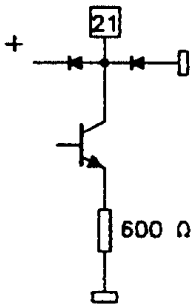
Pin 16: Timing capacitor wideband for DBX
Pin 17: Timing capacitor spectral for DBX



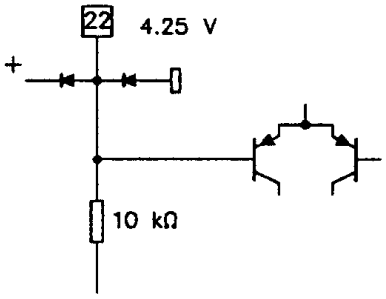
Pin 18: Capacitor wideband for DBX
Pin 19: Capacitor spectral for DBX



Pin 20: Variable emphasis out for DBX

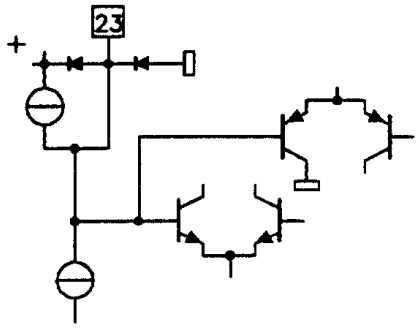


Pin 21: Variable emphasis in for DBX

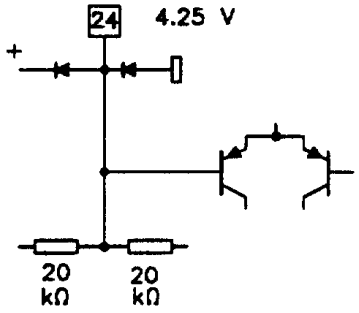


Pin 22: Capacitor noise reduction for DBX

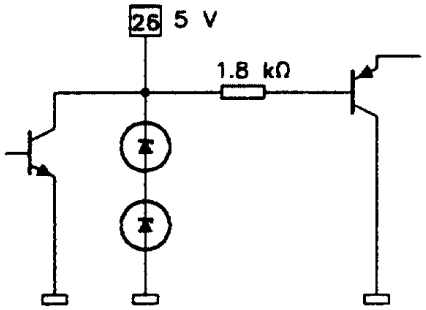
Fig.18 Internal circuits (continued from Fig.17).



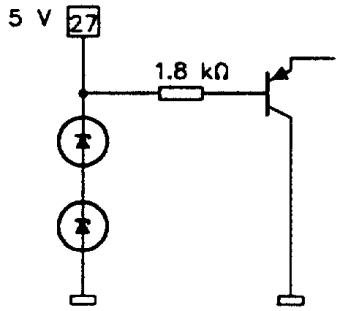
Pin 23: Capacitor mute for SAP



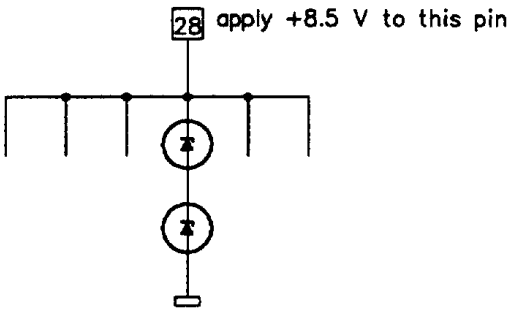
Pin 24: Capacitor DC decoupling for SAP



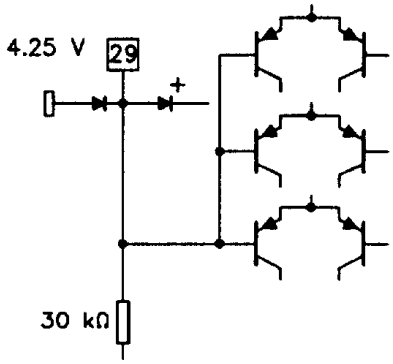
Pin 26: SDA (I²C-bus DATA input/output)



Pin 27: SCL (I²C-bus CLOCK)

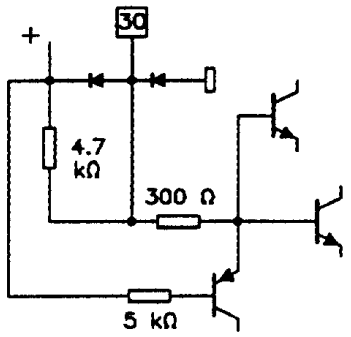


Pin 28: Supply voltage

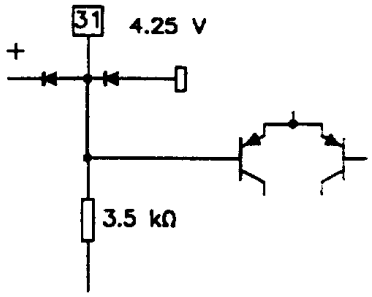


Pin 29: Input composite signal

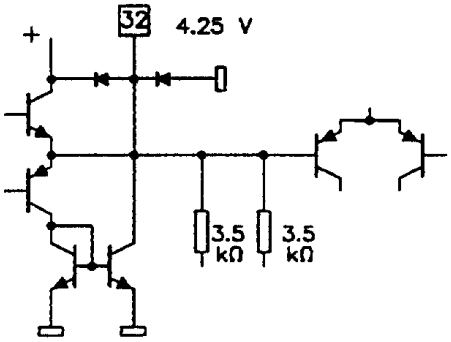
Fig.19 Internal circuits (continued from Fig.18).



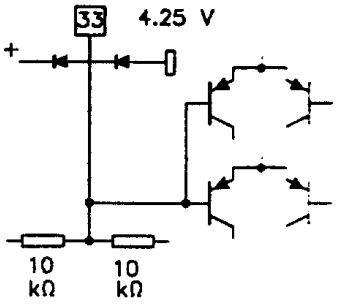
Pin 30: Smoothing capacitor for supply



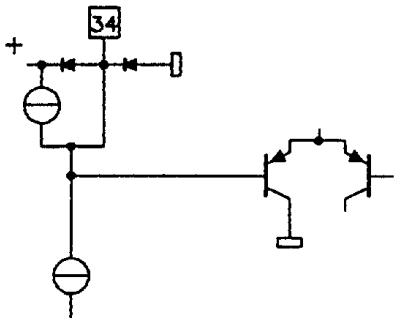
Pin 31: Capacitor for pilot detector



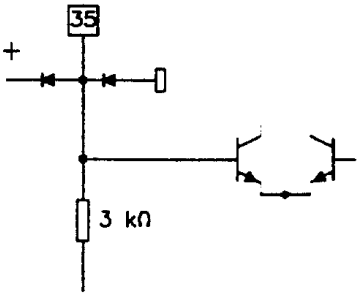
Pin 32: Capacitor for pilot detector



Pin 33: Capacitor for phase detector

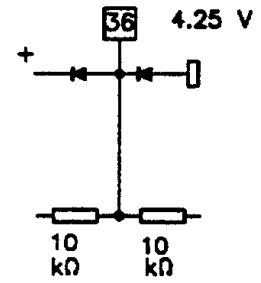


Pin 34: Capacitor for filter adjust

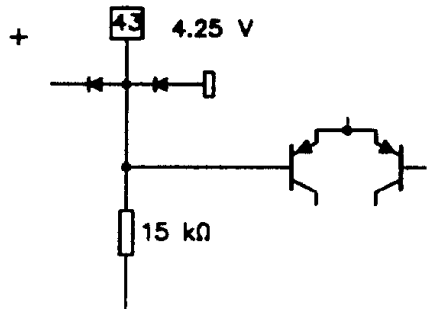


Pin 35: Ceramic resonator

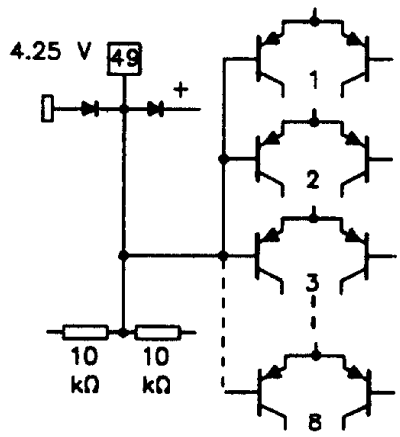
Fig.20 Internal circuits (continued from Fig.19).



Pin 36: Capacitor DC decoupling mono
Pin 37: Capacitor DC decoupling stereo/SAP



Pin 43: Capacitor 1 pseudo function
Pin 42: Capacitor 2 pseudo function

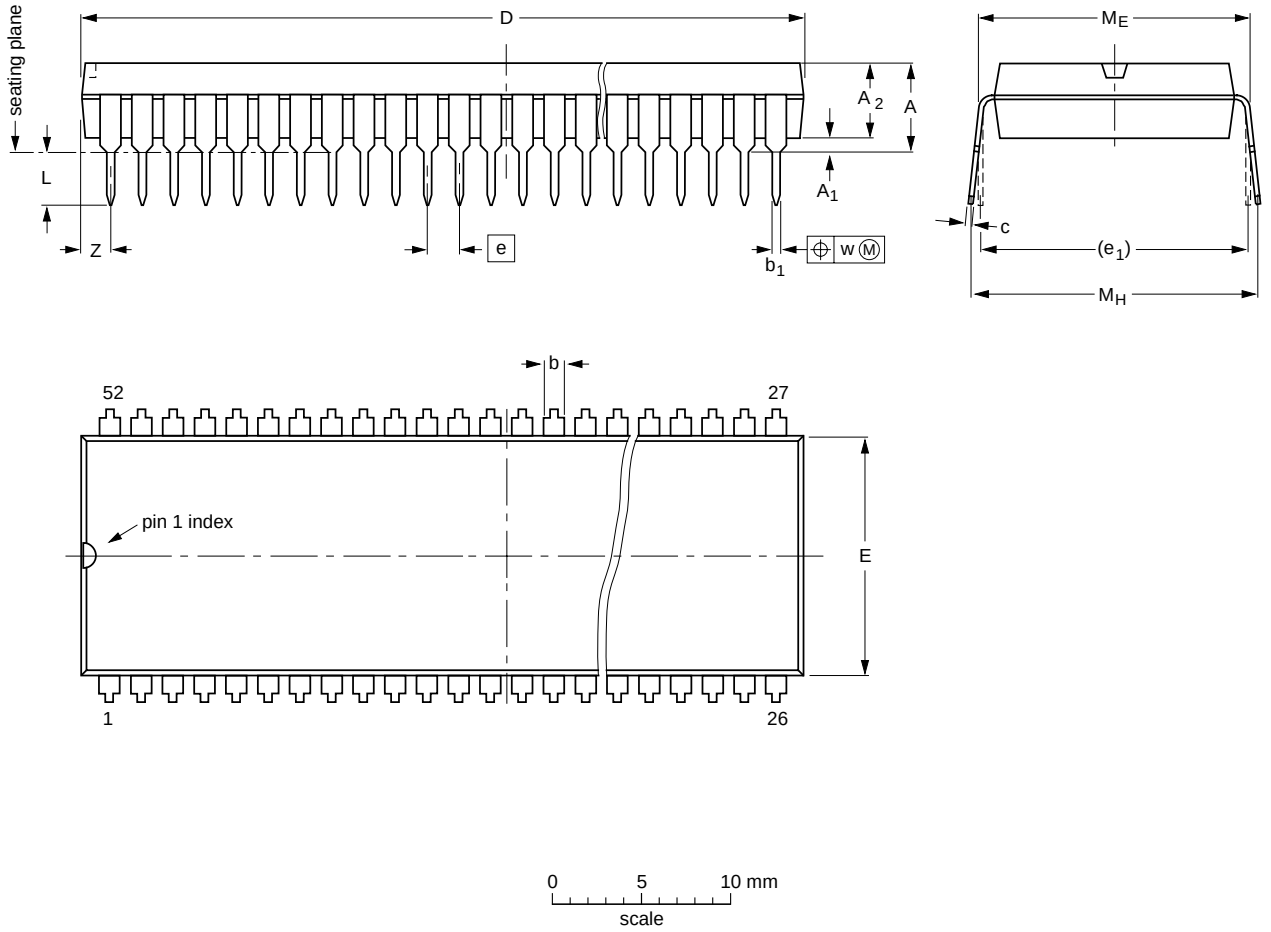


Pin 49: Capacitor subwoofer

Fig.21 Internal circuits (continued from Fig.20).

PACKAGE OUTLINES

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

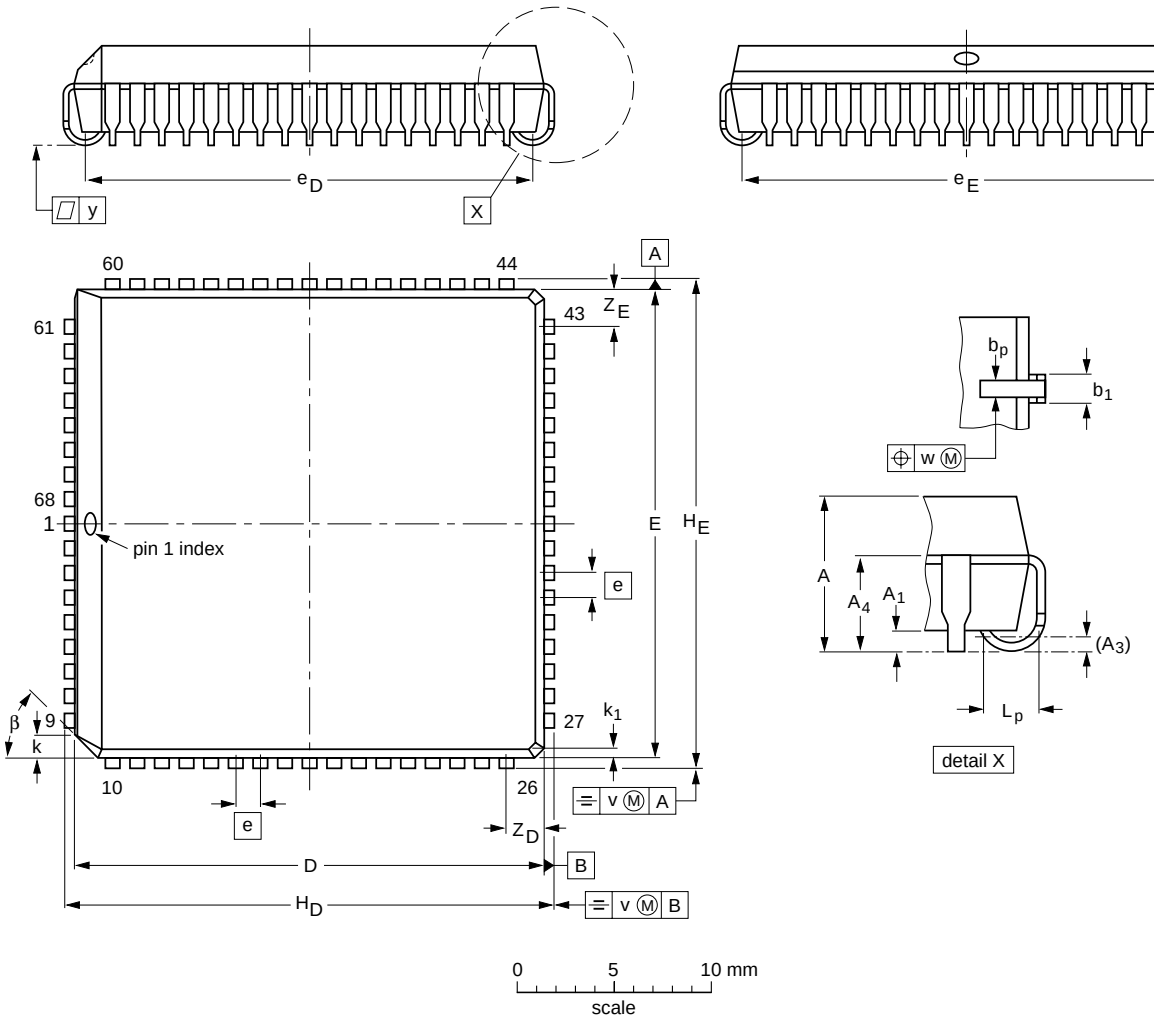
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

SDIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

PLCC

Reflow soldering

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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